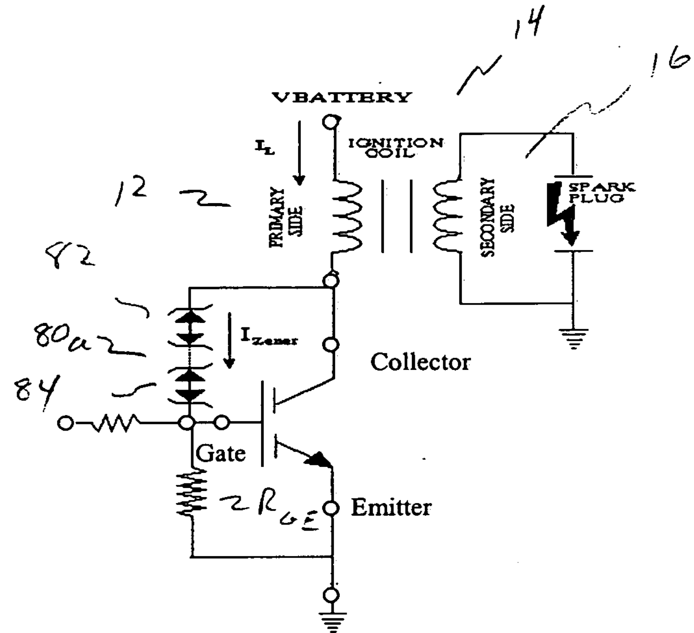


Fig. 1 IGBT with Monolithic or Discrete Diode Collector to Gate Clamp Circuit

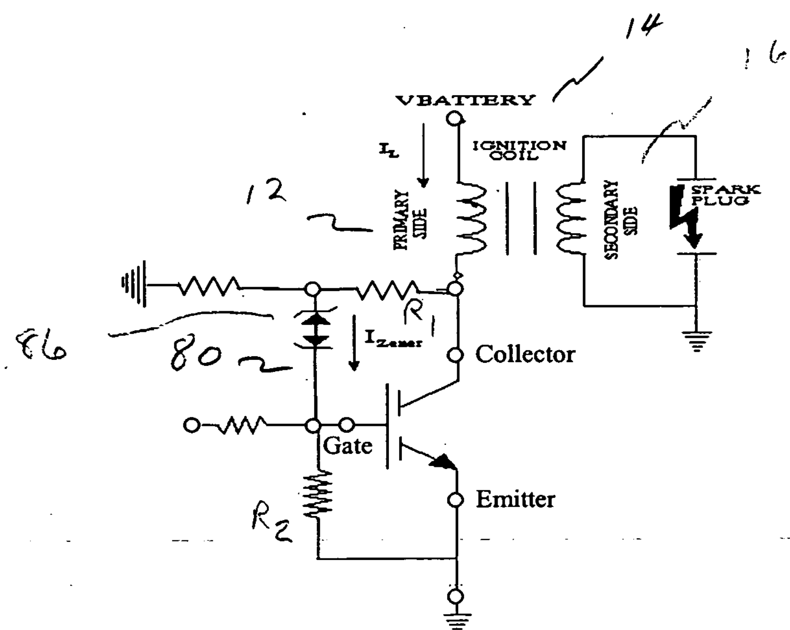


Fig. 2 IGBT with Monolithic or Discrete Resistive Voltage Divider and Diode Collector to Gate Clamp Circuit

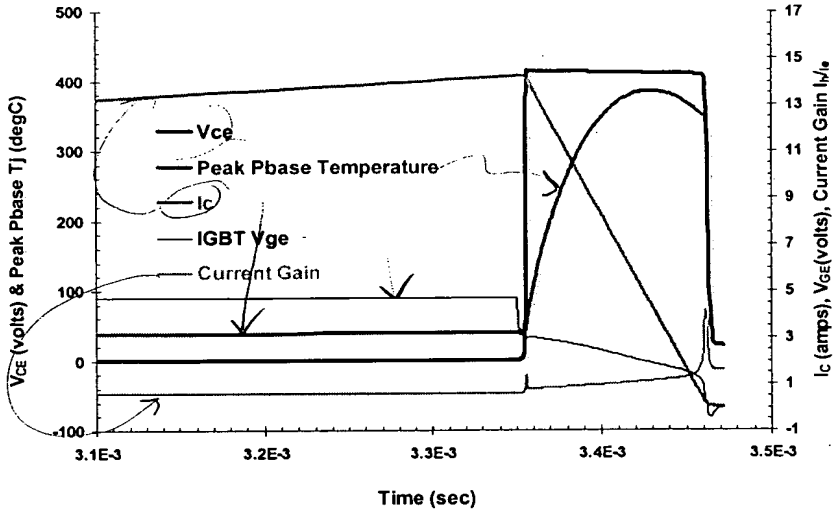


Fig. 3 Simulated 14.2A, 310mJ SCIS stress for and IGBT used in the circuit of Fig 1.

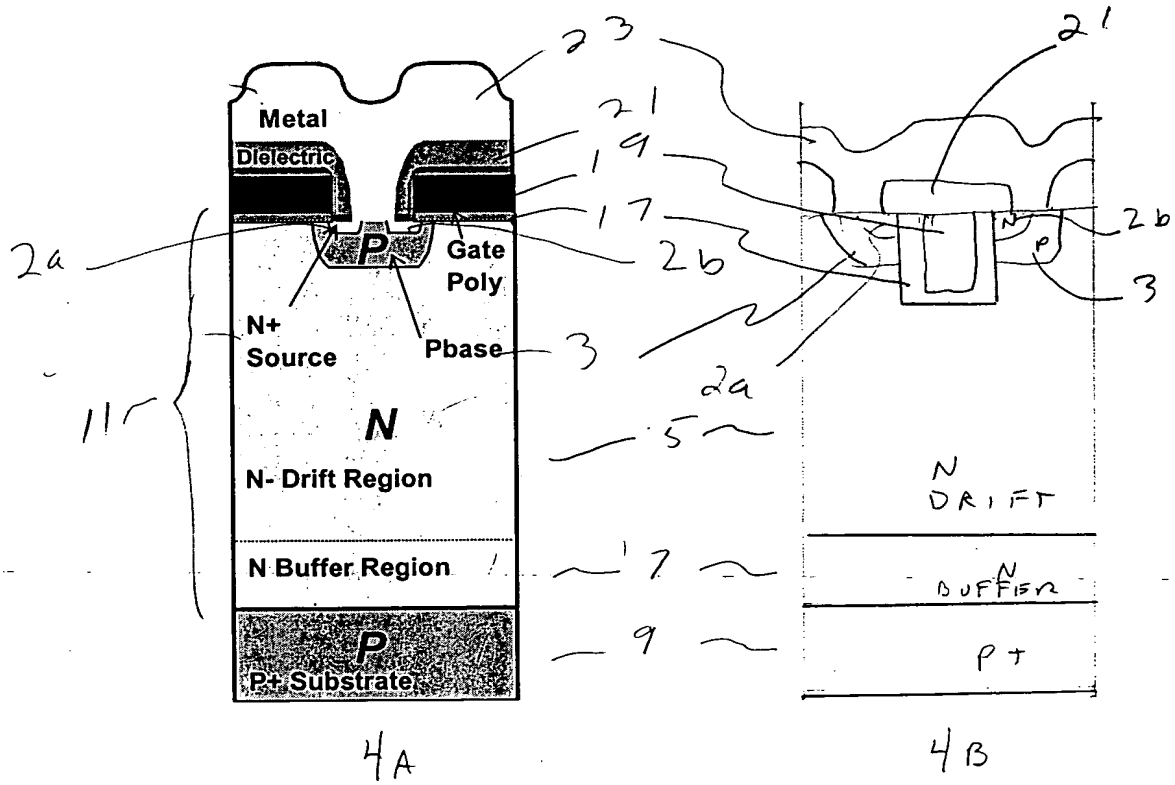
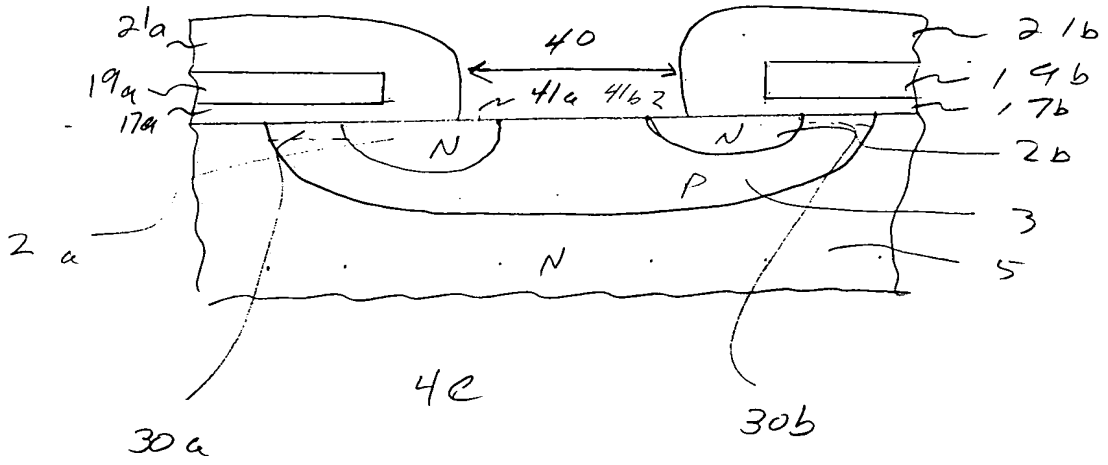
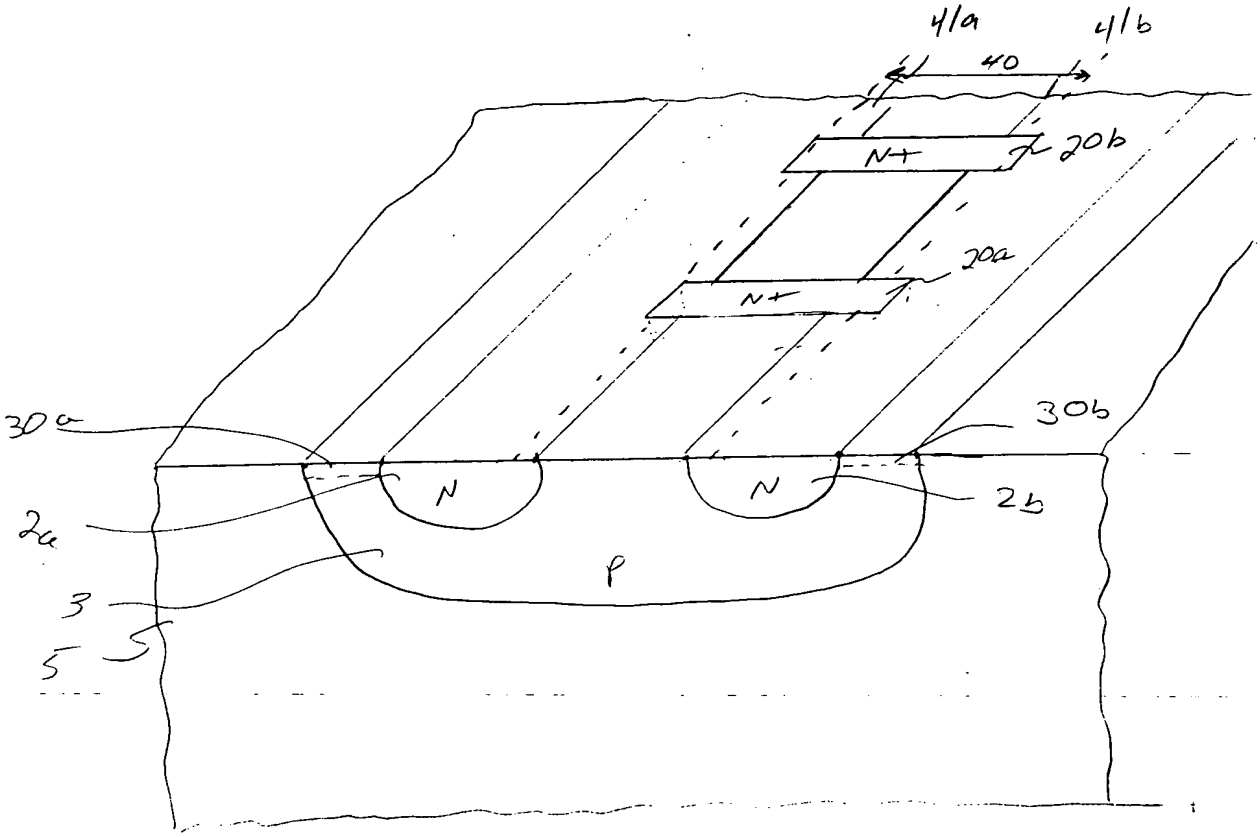


Fig. 4 Typical IGBT stripe cell vertical cross-section .





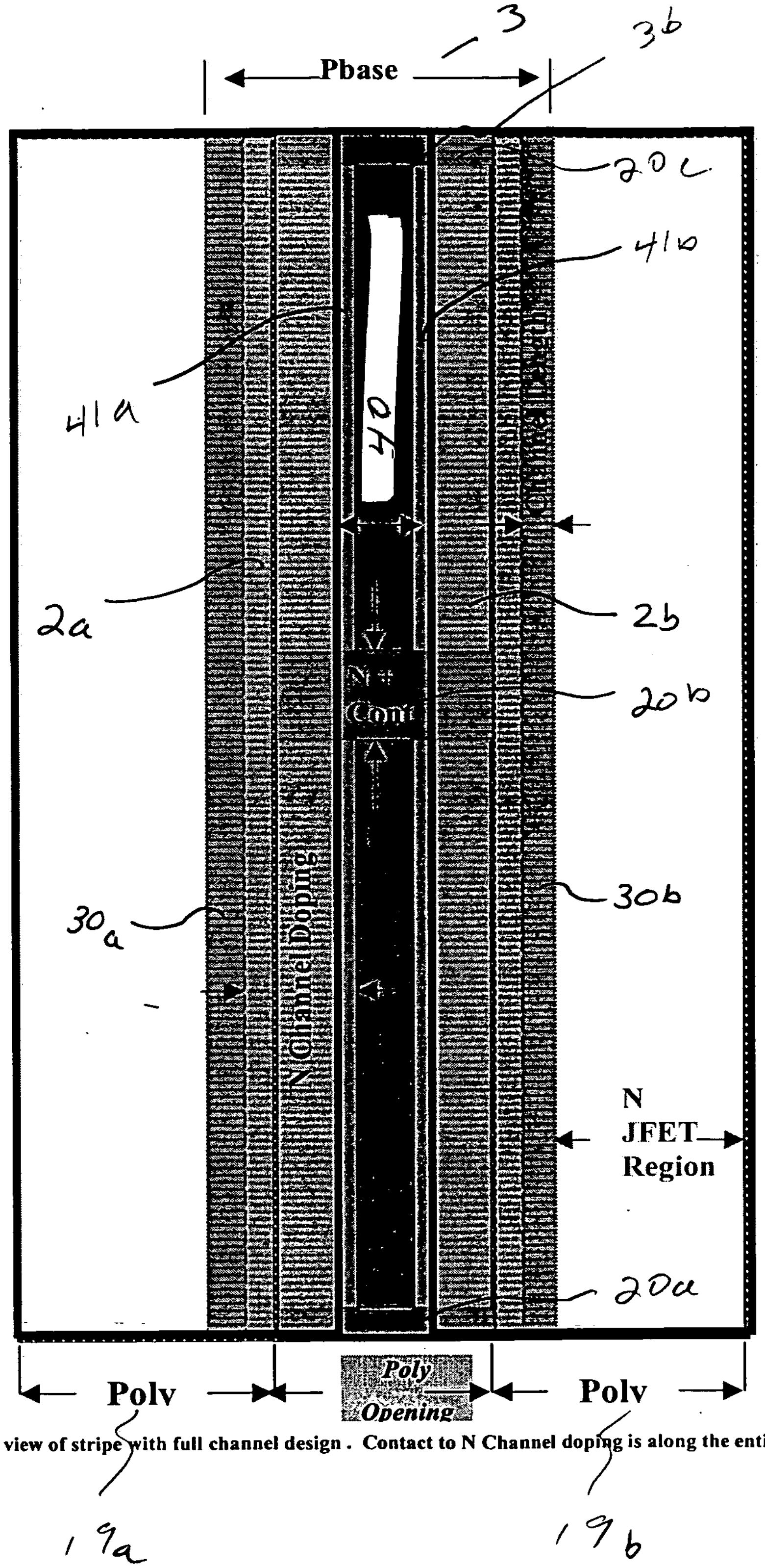


Fig. 5 Top view of stripe with full channel design. Contact to N Channel doping is along the entire length of the stripe.

10055211.012302

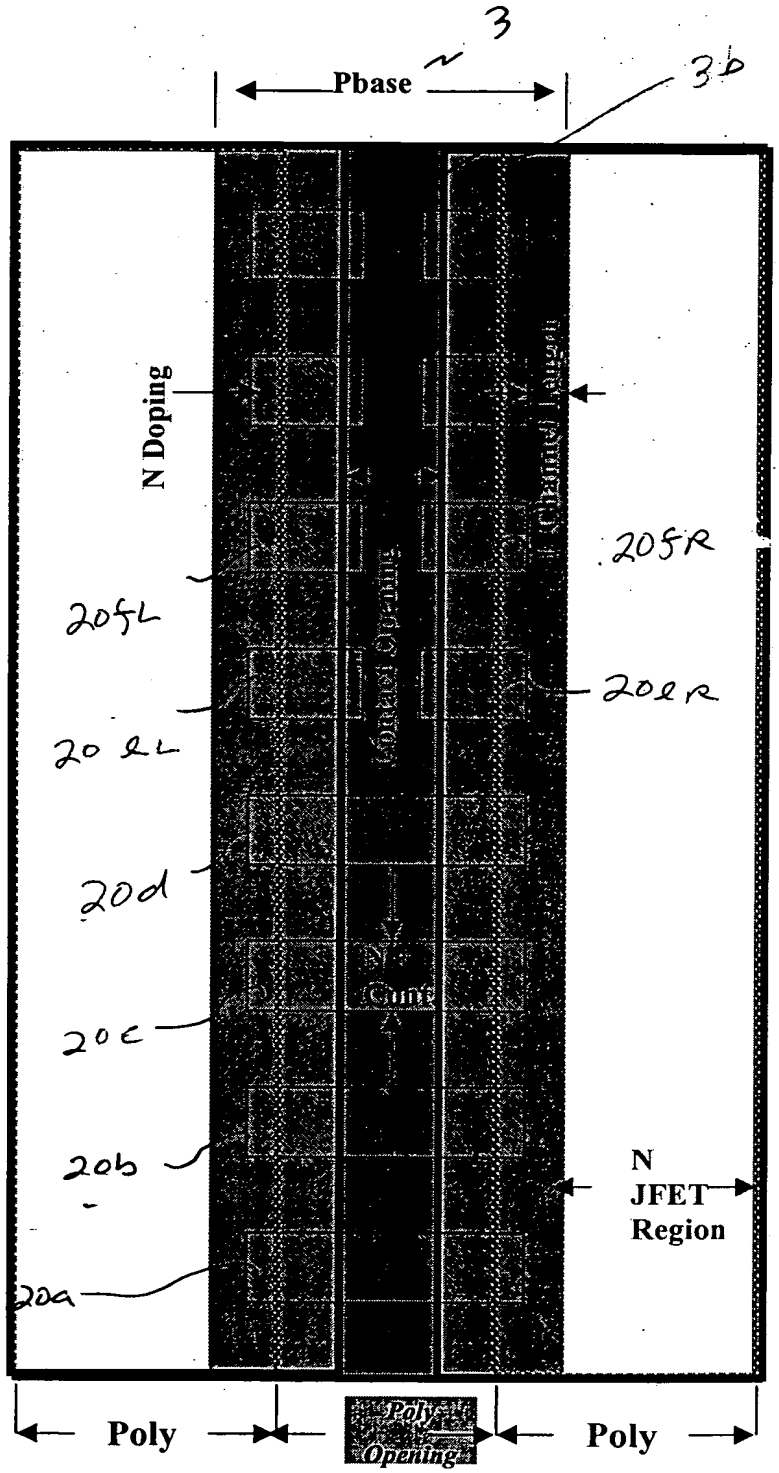


Fig. 6 Top view of stripe with channel version A exclude design. Top half of stripe separate N+ contacts. Bottom half of stripe continuous N+ contacts across the contact opening.

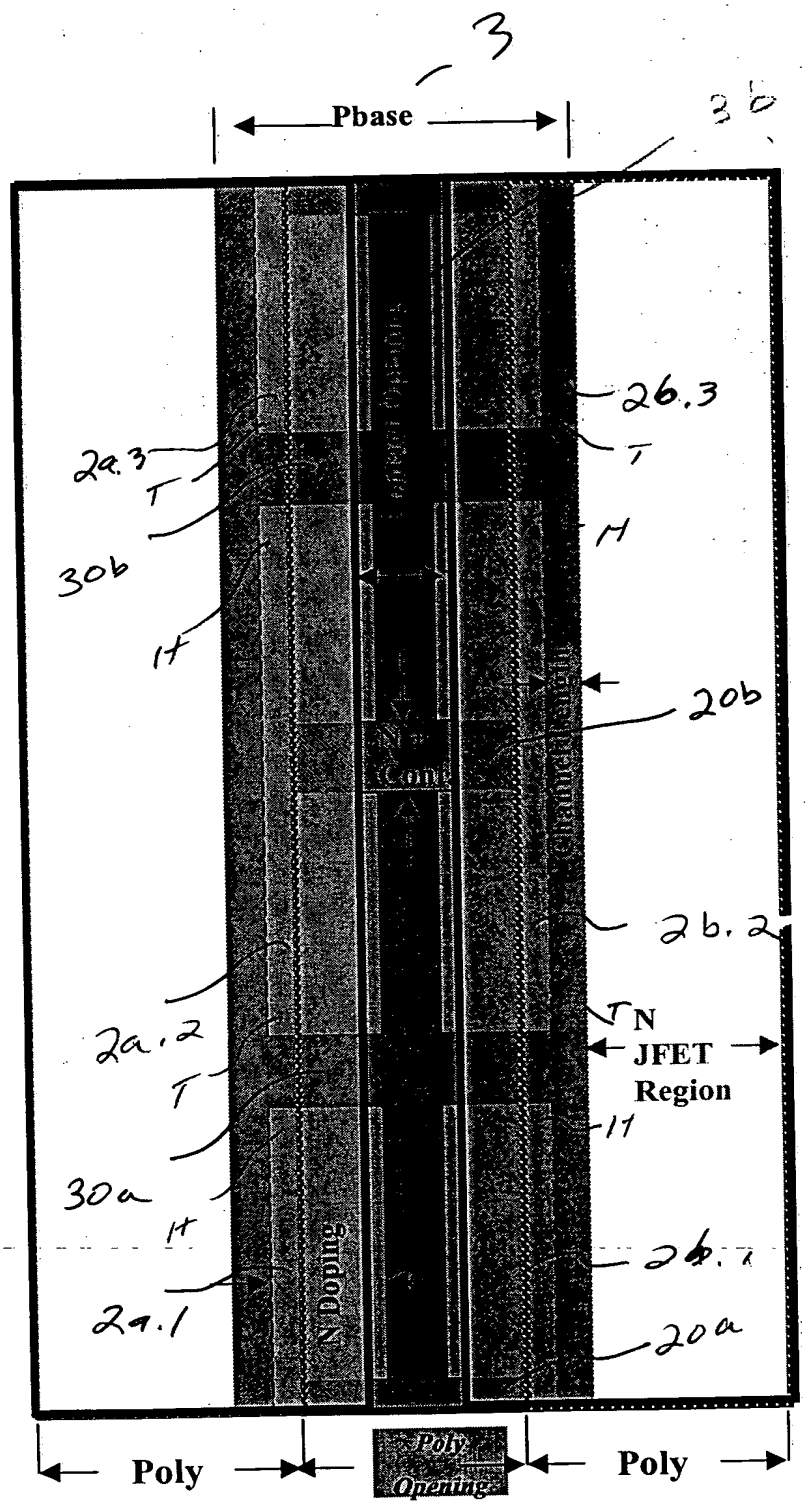


Fig. 7 Top view of stripe with Version B channel exclude design.

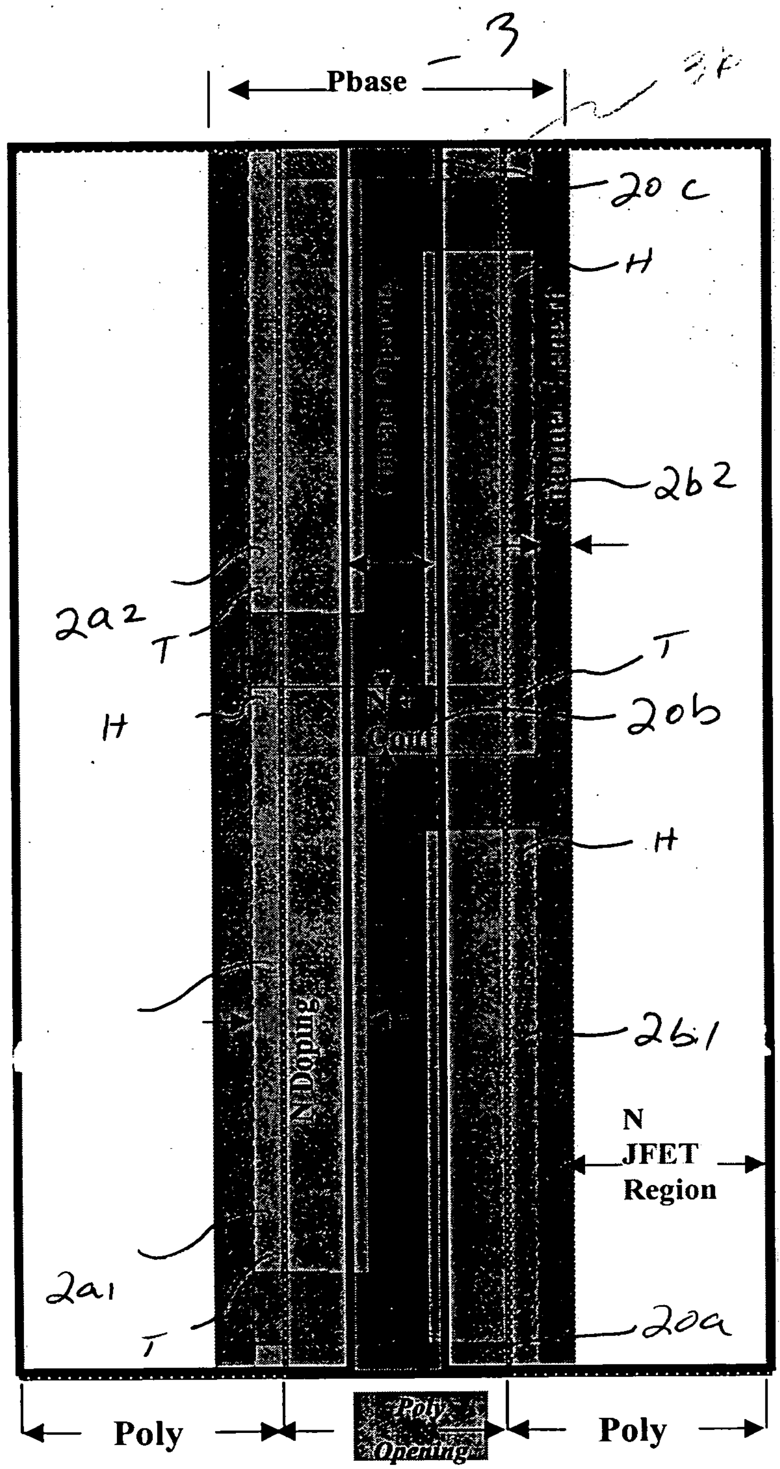


Fig. 8 Top view of stripe with Version C channel exclude design.

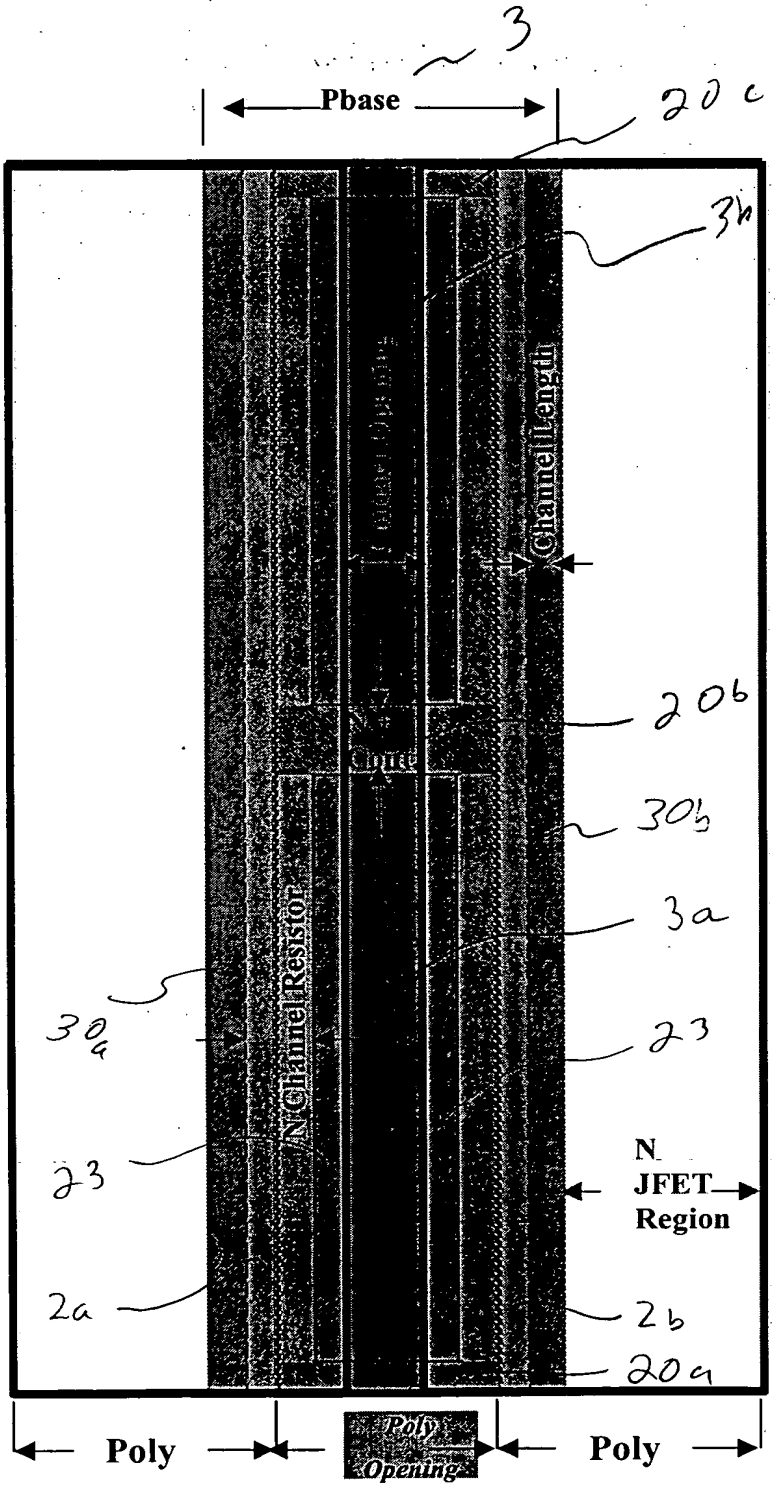


Fig. 9 Top view of stripe with full channel length channel resistor design.

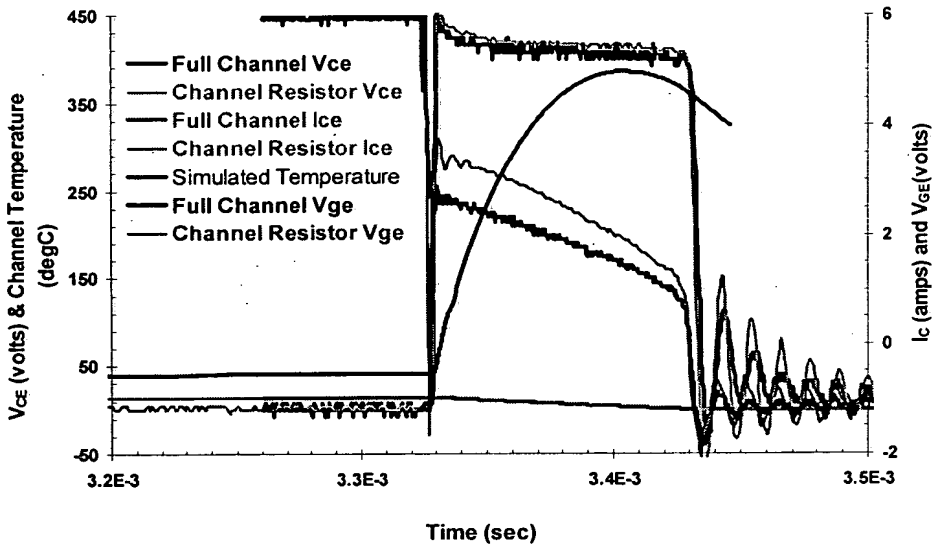


Fig. 10 Measured 27°C, 14.2A, Vge=5V, Rge=1kΩ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with channel resistor having equivalent active area.

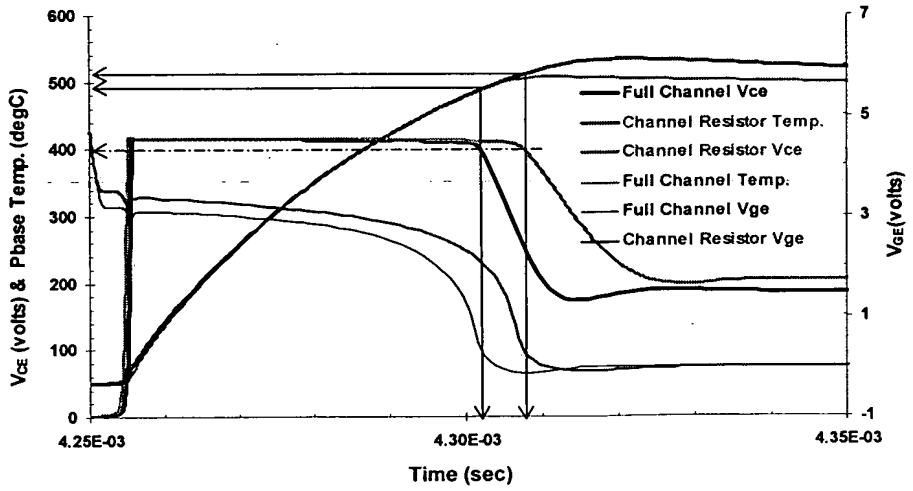


Fig. 11 Simulated 27°C, 17.8A, Vge=5V, Rge=1kΩ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with non-temperature compensated channel resistor having equivalent active area.

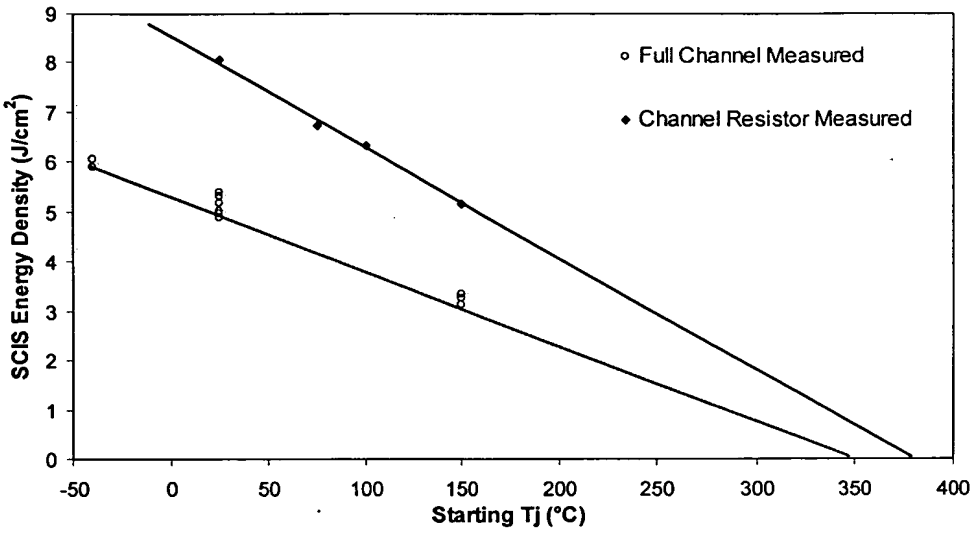


Fig. 12 Measured SCIS energy density capability with primary inductance of 3mH.

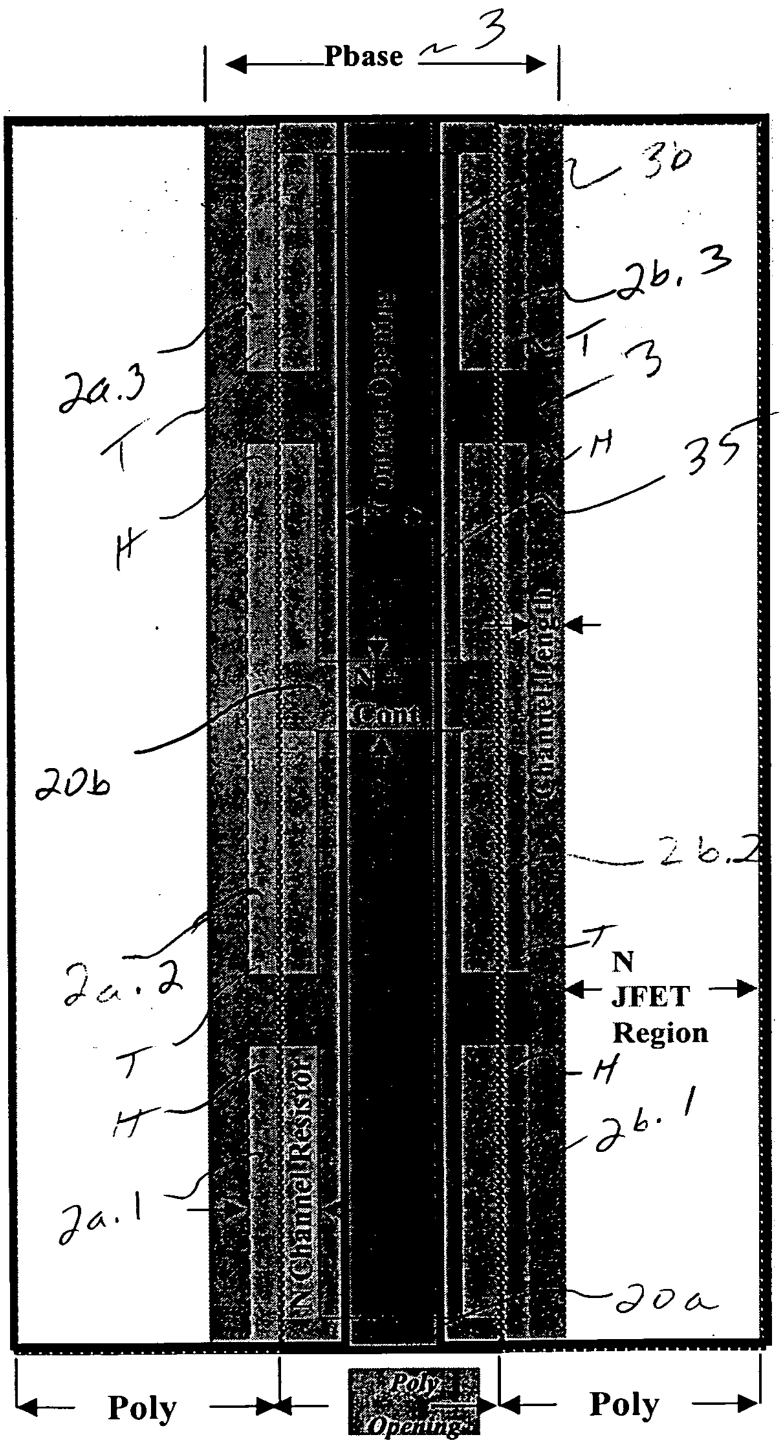


Fig. 13 Top view of stripe "H" pattern channel resistor design.

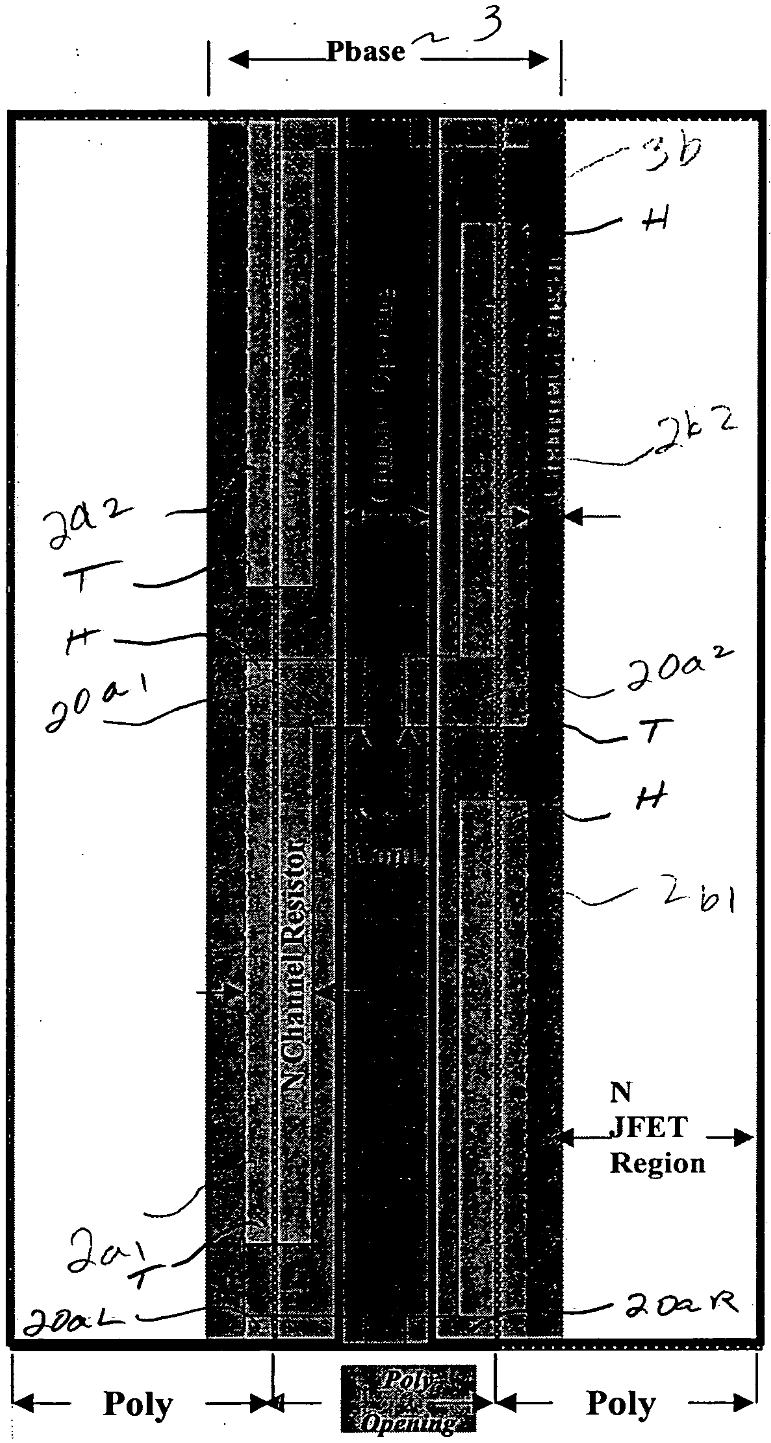


Fig. 14 Top view of stripe "H" pattern channel resistor design.

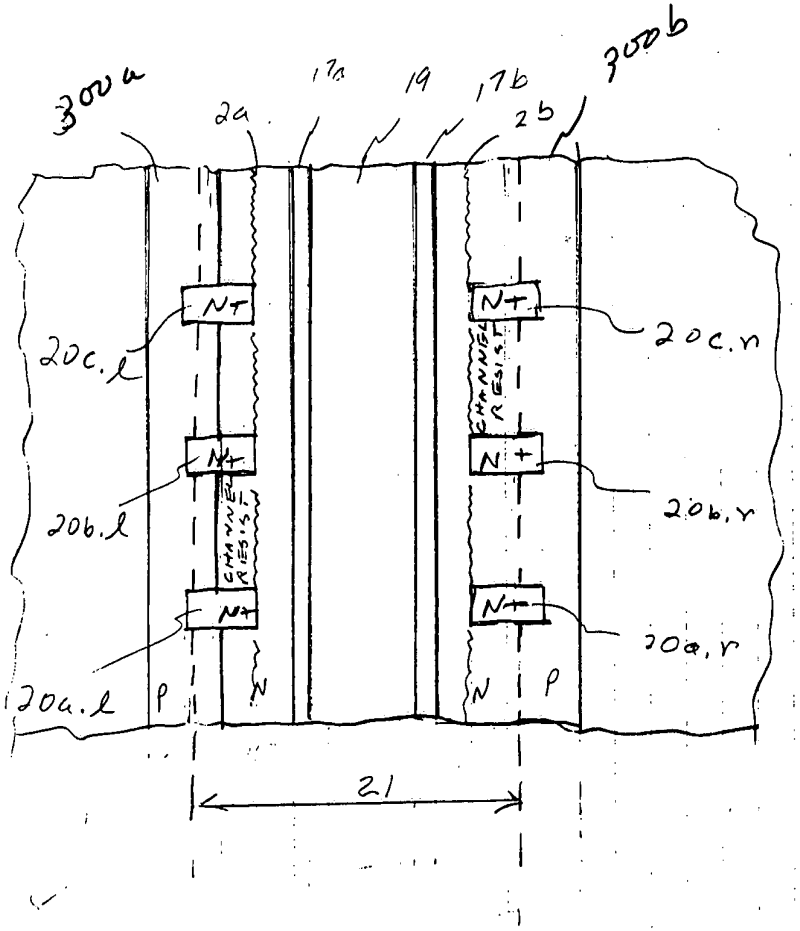

300a
17a
19
17b
300b
2a
2b
20c.ℓ
20c.n
20b.ℓ
20b.r
20a.ℓ
20a.r
CHANNEL REGION
N+
P
N
21

FIG. 15

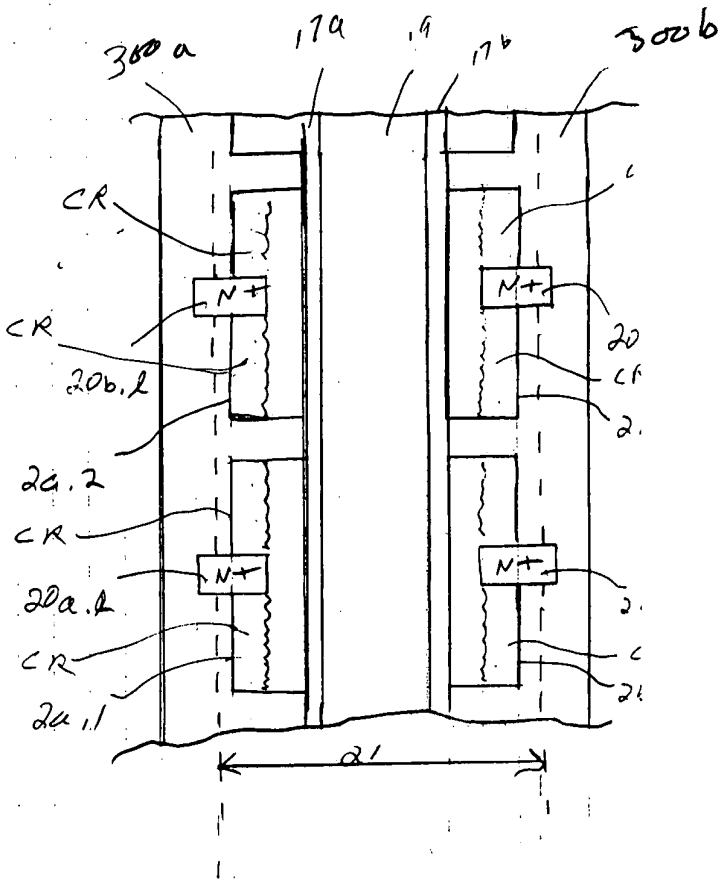
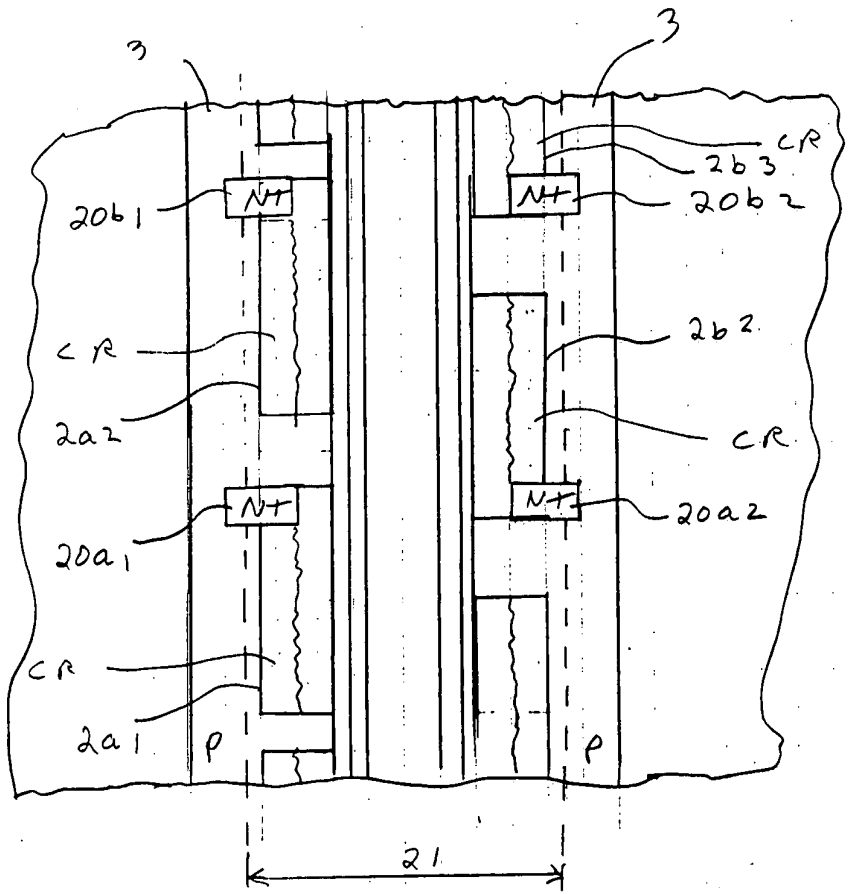

300a
17a
19
17b
300b
CR
20b.ℓ
2a.2
20a.ℓ
2a.1
N+
21

FIG. 16



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